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09/761,217	01/16/2001	Shailender Chaudlhry	SUN-P3900-SPL	4812

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EXAMINER	
O BRIEN, BARRY J	
ART UNIT	**PAPER NUMBER**
2183	5

DATE MAILED: 04/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/761,217	CHAUDLHRY ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment A as received on 2/02/2004.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Response to Arguments

5. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection. See below.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it

> pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 1-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 1, 12 and 23 recite the limitation, "wherein the head thread and all speculative threads execute instructions from separate instruction caches." In the remarks on p.11 of the current amendment, lines 6-11, the Applicant states that, "threads in the present invention to do not share code" and thus, "must provide a separate instruction cache for each thread," citing Figure 1 as the basis for this limitation. However, Figure 1 shows two processors (102 and 104), each with an instruction cache (112 and 120), which are said to be multithreaded, that is allowing multiple threads to execute concurrently (see p.8 lines 5-12 of specification). This implies that each thread executed on one of the processors would, in fact, share the same instruction cache.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marcuello et al., *Value Prediction for Speculative Multithreaded Architectures* (hereinafter Marcuello(1)), and further by Marcuello et al., *Speculative Multithreaded Processors* (hereinafter Marcuello(2)),

incorporated by reference in Section 2 of Marcuello(1), in view of Shiell et al., U.S. Patent No. 5,850,543 (hereinafter Shiell), further in view of Patterson et al., *Computer Organization & Design: The Hardware/Software Interface* (hereinafter Patterson).

10. Regarding claims 1, 12 and 23, taking claim 12 as exemplary, Marcuello has taught an apparatus that facilitates predicting a result produced by a section of code in order to support speculative program execution, the section of code including a plurality of program instructions (see Marcuello(2) Col.1 lines 11-16 and Col.2 line 47 – Col.3 line 9), the apparatus comprising:

a. A head thread that is configured to execute the section of code within a program, wherein executing the section of code produces the result (see Marcuello(2) Col.5 lines 19-25),

b. A prediction mechanism that is configured to generate a predicted result to be used in place of the result before the head thread produces the result (see Marcuello(2) Col.3 lines 2-9),

c. A speculative thread that is configured to speculatively execute subsequent code within the program using the predicted result (see Marcuello(2) Col.3 lines 2-9 and Col.6 lines 14-20), wherein the subsequent code follows the section of code in an execution stream of the program (see Marcuello(2) Col.5 lines 26-29), and wherein speculatively executing the subsequent code involves a speculative looping operation (see Marcuello(1) Col.3 lines 17-43).

d. A determination mechanism that is configured to determine if a difference between the predicted result and the result generated by the head thread affected execution of the speculative thread (see Marcuello(2) Col.4 lines 53-57),

e. A joining mechanism that is configured to merge state associated with the speculative thread with state associated with the head thread if the difference did not affect execution of the speculative thread (see Marcuello(2) Col.4 lines 53 – Col.5 line 5 and Col.5 lines 26-35),

f. Wherein if the difference affected execution of the speculative thread, the apparatus is configured to execute the subsequent code again using the result generated by the head thread (see Marcuello(2) Col.8 lines 7-11).

11. Marcuello has not explicitly taught wherein speculatively executing the subsequent code also involves performing one of:

a. A speculative method invocation to speculatively execute the subsequent code,

b. A speculative function call to speculatively execute the subsequent code,

c. A speculative procedure call to speculatively execute the subsequent code,

12. However, Shiell has taught the speculative execution of non-sequential instructions such as subroutine calls (see Col.8 lines 50-55). One of ordinary skill in the art would have recognized that executing non-sequential instructions speculatively is desirable as it minimizes the degradation of processor performance (see Col.2 lines 19-22). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Marcuello to also execute subroutine calls so that performance degradation is minimized.

13. Furthermore, Marcuello in view of Shiell has taught a microprocessor that executes a thread using a single instruction cache (see Marcuello(1) Fig.1), but has not explicitly taught wherein the head thread and all speculative threads execute instructions from separate instruction caches.

14. However, Patterson has taught multiple processors each executing a thread using instructions from each processor's own instruction cache (see p.717-718). One of ordinary skill in the art would have recognized that having multiple processors, each executing a thread and having its own cache, allows each thread to execute instructions from separate instruction caches, and further provides improved performance over a single processor (see p.712-713). Therefore, one of ordinary skill in the art would have found it obvious to duplicate the processor of Marcuello in view of Shiell to provide multiple processors, each executing a thread using instructions from separate instruction caches, so that performance of the system can be improved.

15. Furthermore, while multiple instruction cache's allowing multiple threads to each use instructions from a different instruction cache is not taught, a single instruction cache allowing a thread to use instructions from it is taught (see Marcuello(1) Fig.1). The limitation of multiple threads using multiple instruction caches performs the same function as duplicating the single thread and single instruction cache, providing no new or unexpected result over the prior art. Therefore, one of ordinary skill in the art would have found it obvious to duplicate the processor executing a thread from a single instruction cache of Marcuello, creating multiple processors each executing a thread from a different instruction cache (see In re Harza, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960)).

16. Claims 1 and 23 are nearly identical to claim 12. Claim 1 differs in its lack of an apparatus to perform its method upon, but encompasses the same scope as claim 12. Claim 23 differs in it claiming a computer-readable storage medium storing instructions that when executed by a computer cause the computer to perform a method, which is taught by Marcuello

(see Marcuello(1) "ICache" of Fig.1), but the method encompasses the same scope as claim 12. Therefore, claims 1 and 23 are rejected for the same reasons as claim 12.

17. Regarding claims 2, 13 and 24, taking claim 13 as exemplary, Marcuello has taught the apparatus of claim 12 as shown above, wherein while executing the subsequent code again, the apparatus is configured to perform a rollback operation for the speculative thread to undo actions performed by the speculative thread (see Marcuello(2) Col.8 lines 7-11).

18. Claims 2 and 24 are nearly identical to claim 13. They differ in their parent claims, but encompass the same scopes. Therefore, claims 2 and 24 are rejected for the same reasons as claim 13.

19. Regarding claims 3 and 14, taking claim 14 as exemplary, Marcuello has taught the apparatus of claim 12 as shown above, wherein the determination mechanism is configured to determine if the speculative thread accessed the predicted result. Here, Marcuello has taught the comparing of the results of the head thread and the speculative thread, and either rolling back the speculative thread to be re-executed if the results were not equal (see Marcuello(2) Col.8 lines 7-11), or committing the thread if the results were the same (see Marcuello(2) Col.4 lines 53-57). The Applicant's specification describes this problem of a memory element having been read by the speculative result when it should have first been written by the head thread, causing erroneous results, and consequently either rolling back the speculative thread so it can be re-executed if there was a problem, or committing the thread if there was no problem (p.10 lines 3-23 of the specification). Therefore, Marcuello is inherently operating in the same manner as the claim language has stated, in that if the speculative thread incorrectly reads the result of a write

operation, it would produce erroneous results that would be detected in the thread comparison of Marcuello and consequently perform the correct action.

20. Claim 3 is nearly identical to claim 14, differing in its parent claim, but encompassing the same scope. Therefore, claim 3 is rejected for the same reasons as claim 14.

21. Regarding claims 4 and 15, taking claim 15 as exemplary, Marcuello has taught the apparatus of claim 12 as shown above, wherein the determination mechanism is configured to determine if the predicted result differs from the result generated by the head thread (see Marcuello(2) Col.4 lines 53-57).

22. Claim 4 is nearly identical to claim 15, differing in its parent claim, but encompassing the same scope. Therefore, claim 4 is rejected for the same reasons as claim 15.

23. Regarding claims 5 and 16, taking claim 16 as exemplary, Marcuello has taught the apparatus of claim 12 as shown above, wherein the prediction mechanism is configured to generate the predicted result by looking up a value based upon a program counter for the program (see Marcuello(1) Col.7 lines 14-20).

24. Claim 5 is nearly identical to claim 16, differing in its parent claim, but encompassing the same scope. Therefore, claim 5 is rejected for the same reasons as claim 16.

25. Regarding claims 6 and 17, taking claim 17 as exemplary, Marcuello has taught the apparatus of claim 16 as shown above, wherein the prediction mechanism is configured to generate the predicted result by additionally looking up the valued based upon at least one previously generated value for the result (see Marcuello(1) Col.5 lines 22-38).

26. Claim 6 is nearly identical to claim 17, differing in its parent claim, but encompassing the same scope. Therefore, claim 6 is rejected for the same reasons as claim 17.

27. Regarding claims 7 and 18, taking claim 18 as exemplary, Marcuello has taught the apparatus of claim 16 as shown above, wherein the prediction mechanism is configured to generate the predicted result by performing a function on the value (see Marcuello(1) Col.5 lines 28-31).

28. Claim 7 is nearly identical to claim 18, differing in its parent claim, but encompassing the same scope. Therefore, claim 7 is rejected for the same reasons as claim 18.

29. Regarding claims 8 and 19, taking claim 19 as exemplary, Marcuello has taught the apparatus of claim 12 as shown above, wherein the section of code includes one of, a method, a function, and a procedure (see Marcuello(1) Col.3 lines 24-33).

30. Claim 8 is nearly identical to claim 19, differing in its parent claim, but encompassing the same scope. Therefore, claim 8 is rejected for the same reasons as claim 19.

31. Regarding claims 9 and 20, taking claim 20 as exemplary, Marcuello has taught the apparatus of claim 12 as shown above, wherein the section of code is a body of a loop in the program, and the result is a loop carried dependency for the loop (see Marcuello(1) Col.4 line 37 – Col.5 line 7).

32. Claim 9 is nearly identical to claim 20, differing in its parent claim, but encompassing the same scope. Therefore, claim 9 is rejected for the same reasons as claim 20.

33. Regarding claims 10 and 21, taking claim 21 as exemplary, Marcuello has taught the apparatus of claim 12, further comprising a mechanism that performs write operations for the head thread, the mechanism being configured to:

a. Perform a write operation to a primary version of a memory element,

b. Check status information associated with the memory element to determine if the memory element has been read by the speculative thread,

c. Cause the speculative thread to roll back so that the speculative thread can read a result of the write operation if the memory element has been read by the speculative thread,

d. Perform the write operation to a space-time dimensioned version of the memory element if the space-time dimensioned version exists and if the memory element has not been read by the speculative thread.

34. Here, Marcuello has taught the comparing of the results of the head thread and the speculative thread, and either rolling back the speculative thread to be re-executed if the results were not equal (see Marcuello(2) Col.8 lines 7-11), or committing the thread if the results were the same (see Marcuello(2) Col.4 lines 53-57). The Applicant's specification describes this problem of a memory element having been read by the speculative result when it should have first been written by the head thread, causing erroneous results, and consequently either rolling back the speculative thread so it can be re-executed if there was a problem, or committing the thread if there was no problem (p.10 lines 3-23 of the specification). Therefore, Marcuello is inherently operating in the same manner as the claim language has stated, in that if the speculative thread incorrectly reads the result of a write operation, it would produce erroneous results that would be detected in the thread comparison of Marcuello and consequently perform the proper action.

35. Claim 10 is nearly identical to claim 21, differing in its parent claim, but encompassing the same scope. Therefore, claim 10 is rejected for the same reasons as claim 21.

36. Regarding claims 11 and 22, taking claim 22 as exemplary, Marcuello has taught the apparatus of claim 21 as shown above, wherein the joining mechanism is configured to:

a. Merge the space-time dimensioned version of the memory element into the primary version of the memory element (see Marcuello(2) Col.5 lines 2-5),

b. Discard the space-time dimensioned version of the memory element (see Marcuello(2) Col.8 lines 31-46).

37. Claim 11 is nearly identical to claim 22, differing in its parent claim, but encompassing the same scope. Therefore, claim 11 is rejected for the same reasons as claim 22.

Conclusion

38. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

40. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
3/31/2004

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